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High Resolution Electronic Measurements in Nano-Bio Science

ANALOG VS DIGITAL LOCK-IN PROCESSING Francesco Zanetto

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Analog vs digital lock-in processing

- Lock-in amplifiers are commonly divided into analog and digital instruments.
- <u>Both classes of instruments require ADCs and DACs to be implemented, the difference stands in how the demodulation process is carried out.</u>
- Analog LIAs perform the demodulation in the analog domain and digitize the low frequency output of the mixer.
- Digital LIAs digitize the high frequency signal and then demodulate it in the digital domain.



Pro & cons of analog and digital lock-in amplifiers

Analog

<u>PROS</u>

- By changing only the front-end amplifier and mixer, any stimulation frequency can be used.
- It does not require fast ADCs and digital signal processing.
- Simple implementation even in integrated circuits.

<u>CONS</u>

 Sensitive to 1/f noise of any stage after the demodulation (mixer, further gain stages, ...)

<u>PROS</u>

• Insensitive to 1/f noise of its building blocks.

Digital

- It can achieve sub-ppm resolution.
- Less components are required.

<u>CONS</u>

- Fast ADCs and complex digital signal processing are required.
- Implementation in ICs is not trivial, especially for high stimulation frequencies.

Analog lock-in structure



- An (optional) high-pass filter can be used to remove the DC component before the demodulation.
- Two acquisition chains are needed after the TIA to perform I/Q demodulation and fully reconstruct the DUT impedance.
- A low-pass filter is used to avoid aliasing effects in the ADC acquisition, further lowpass filtering can be done digitally to reduce the readout bandwidth if needed.

Requisite for using analog lock-in amplifiers

- The analog lock-in amplifier has the same noise performance as the digital one if the readout bandwidth is sufficiently larger than the 1/f noise corner frequency of the overall circuit.
- This ensures that the 1/f contribution is negligible with respect to the white noise.
- <u>As a rule of thumb, the readout</u> <u>bandwidth should be roughly 10</u> <u>times larger than the 1/f noise corner</u> <u>frequency.</u>



$$\frac{1/f}{f_{BW}} = 1 MHz \quad \rightarrow v_N^2 = 1.6 \cdot 10^{-12} + 10^{-10}$$

$$f_{BW} = 100 kHz \quad \rightarrow v_N^2 = 1.38 \cdot 10^{-12} + 10^{-11}$$

$$f_{BW} = 10 kHz \quad \rightarrow v_N^2 = 1.15 \cdot 10^{-12} + 10^{-12}$$

Generation of the lock-in signals

- <u>The stimulation chain can be a source of noise in the measurement.</u> Make sure to choose the right components not to worsen the lock-in performance.
- The stimulation and I/Q demodulation signals are usually generated with a direct digital synthesizer (DDS).



Increasing the number of samples per sinusoid period improves the spectral purity of the stimulation signal and allows to better filter out the spurious harmonics.



Mixer

- The mixer is critical in setting the lock-in amplifier performance because any nonideality is directly translated into a measurement error.
- <u>It should have output offset and 1/f noise as low as possible</u> and sufficiently high bandwidth and linearity (in the case of sinusoidal multipliers).

Passive mixer

 Low 1/f noise, only square wave demodulation



Active mixer

• Higher 1/f noise, more complex but sinusoidal demodulation possible.



Mixer non-idealities

- <u>Measurement errors introduced by the mixer cannot be removed because the signal has already been moved to low frequency.</u>
- Try to make the mixer work always in the same operating conditions (for example, remove DC offset before the demodulation) to avoid signal-dependent errors.

Example: DC offset at mixer input can translate into demodulation error



Amplification after the mixer

- If further amplification is needed after the mixer, choose an amplifier with very low 1/f noise corner frequency and offset, because they are summed directly to the signal to be measured and can't be removed afterwards.
- Chopper-stabilized amplifiers are a good option, because they are specifically designed for these applications.



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Analog to digital conversion

- A slow ADC is enough to digitize and acquire the lock-in output, that is already a DC signal.
- <u>Choose the ADC number of bits such that</u> <u>the LSB is much smaller than the RMS noise</u> <u>at the input of the converter.</u>
- This guarantees that the measurement result is not affected by the A/D conversion.
- Oversampling (choosing f_{SAMP} >> BW_{READOUT}) can be used to make the effect of the ADC quantization noise negligible on the measurement result.



Digital signal processing

- A digital processor is used to control the ADC operations, acquire the conversion result and provide it to the user.
- Usually a standard microcontroller (Arduino, STM32, ...) is enough to perform this tasks since all the operations are performed at low speed (tens of kHz).
- A digital low-pass filter (such as a moving average filter) can be implemented on the microcontroller to further reduce the readout bandwidth and increase the measurement accuracy if needed.





M. Giacometti et al., IEEE TBIOCAS, vol. 16, no. 6, pp. 1325-1336 (2022)

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Ni micropillar

 The malaria parasite infects red blood cells (RBC) and makes them magnetic by producing hemozoin crystals.

- This property can be used to develop a system-on-chip for malaria detection.
- Healthy cells sediment on the bottom of the chip while infected ones are captured with a magnet.
- The infected cells are detected by using impedance sensing electrodes.

Example of application: detection of malaria infections



Example of application: detection of malaria infections





Differential electrodes to limit the effect of temperature fluctuations of the liquid.



- The measurement accuracy is limited by the conductivity fluctuations of the liquid.
- A low-cost analog lock-in amplifier can be used to perform the impedance measurement at 1 MHz.

Example of application: detection of malaria infections



- Custom biochip with 91 differential electrodes in parallel for large sensing area.
- Successful detection down to 40 infected cells per µL of buffer solution.
- By optimizing the biochip layout, single cell detection can also be achieved at the price of a smaller sensing area.





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Digital lock-in structure



- The front-end circuit is the same as in an analog LIA, but a fast ADC is now required to correctly sample the high-frequency input signal.
- A single acquisition chain is needed, the I/Q processing is performed only in the digital domain → <u>advantage in terms of area with respect to analog LIA.</u>
- The 1/f noise and offset of the acquisition chain do not affect the measurement because the down-conversion is performed in the digital domain.

Digital signal processing (DSP)

- A digital processor is needed to demodulate and filter the ADC readout.
- Especially when the lock-in is operated at high frequencies (tens of MHz), a microcontroller is not enough to perform real-time digital processing \rightarrow <u>FPGA-based</u> <u>digital LIAs are the most common approach.</u>
- The DSP chain operates at the same frequency as the ADC sampling \rightarrow for practical limitations of most FPGAs, it's hard to work at sampling rates above 100 MHz.



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Suppression of the demodulation harmonics

The low-pass filter after the digital mixer has two main functions:

- Define the lock-in readout bandwidth.
- Suppress the harmonics generated by the demodulation process below the RMS noise level of the acquisition chain.



- Depending on the stimulation frequency and required readout bandwidth, the LPF can have challenging specifications in terms of out-of-band attenuation.
- A HPF before the mixer slightly the relaxes the LPF specs by removing the DC offset before it gets upconverted to f_{AC} by the mixer.

Example:

 $V_{IN} = 2V_{pp}$, $V_{noise,RMS} = 10 \,\mu V \rightarrow required LPF attenuation: >>50000$

 f_{AC} = 100 kHz, BW = 1 kHz \rightarrow a first-order LPF provides an attenuation of only 200

- <u>Complex high-order filters, requiring multiple digital adders and multipliers, are</u> <u>usually needed to completely suppress the high-order harmonics.</u>
- In real implementations, this is not always possible because of the limited hardware resources of standard FPGAs.

Is there a better way to remove the harmonics by taking advantage of the fact that we know their frequency a priori?

Cascaded integrator-comb filter

- A cascaded integrator-comb filter is an efficient hardware implementation of the moving average filter.
- <u>It is characterized by notches in its transfer</u> <u>function, that can be set by the user by</u> <u>properly designing the filter structure.</u>
- <u>The notches can be conveniently</u> <u>positioned to completely suppress the</u> <u>demodulation harmonics without requiring</u> <u>many hardware resources.</u>
- A first-order standard LPF can then be used just to define the readout bandwidth.

$$f_{NOTCH} = f_S/N*D$$



Example of application: detection of multiple DNA targets

- Lab-on-chip with functionalized electrodes for simultaneous detection of multiple DNA targets.
- Differential measurement for rejection of all common mode signals by using non-functionalized electrodes.



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2<u>00 μm</u>

Reference sens

Custom digital lock-in amplifier



(Dimensions: 18 cm x 22 cm)

- <u>Compactness and portability</u>
 → Point Of Care configuration
- <u>8 independent channels for multisensing</u>

 → Simultaneous detection of multiple
 biological targets in a single experiment
- Impedance readout resolution of 100 ppm
 →Digital counting of targets
- <u>Stabilization of the chip temperature with</u> <u>m°C accuracy</u>
 - → Stable temperature during the experiment

Detection of target DNA sequences



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ADC requirements for high-speed (> 1 MHz) digital LIAs

- To meet the resolution and speed requirements of certain applications, ADCs with 12 to 16 bits and up to ~100 MSps are usually required.
- This generates a great amount of data that need to be transmitted to the digital processor (e.g: 80 Msps, 14 bit → 1.12 Gbit/s).
- In order not to require clocks in the GHz range, high-speed ADCs usually have a parallel digital interface at the output.

Digital LIAs with many channels in parallel are hard to be implemented because a huge number of digital lines are needed.



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Hybrid lock-in solutions

- The design of multichannel high-speed lock-in acquisition systems is challenging because a good compromise between performance, complexity and area occupation needs to be found.
- Digital LIAs offer excellent performance and low area occupation for the front-end circuit, but they require fast ADCs with a good number of bits.
- This introduces a complexity overhead, because a lot of high-speed digital connections need to be managed.
- In addition, digital LIAs cannot be easily operated above ~100 MHz

Is there a way to keep the advantages of digital LIAs while using slow ADCs as in analog implementations?

Heterodyne lock-in detection

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- An analog mixer moves the signal from high frequency to an intermediate frequency.
- The intermediate frequency should be chosen above the 1/f noise corner of the acquisition circuit in order not to degrade the lock-in performance.
- A single slow ADC can be used to digitize the signal at intermediate frequency, without requiring complex handling of high-speed digital signals.
- A second I/Q demodulation is performed digitally to complete the lock-in acquisition.



Frequency behaviour



- The effect of 1/f noise and offset of all stages is canceled!
- Synchronization of the lock-in processing is needed to ensure consistency!!!

Some math



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Lock-in synchronization: DDS

To ensure consistency of the lock-in processing among different experiments:

- Use the same clock to drive all the DDSs.
- Compute the frequency word of the intermediate DDS as difference between the other two, to avoid rounding approximations:

$$FW_{STIM} = f_{STIM} \cdot \frac{2^{N_{BIT},DDS}}{f_{CLOCK}} \qquad FW_{MID} = f_{MID} \cdot \frac{2^{N_{BIT},DDS}}{f_{CLOCK}}$$

 $FW_{STIM-MID} = FW_{STIM} - FW_{MID}$

• <u>Always start/stop/update all the DDS simultaneously</u> to keep same initial conditions.



Lock-in synchronization: ADC

- The synchronization of the ADC conversion is also critical to obtain consistent results among different experiments.
- <u>Sampling the input waveforms in different points results in different demodulation</u> results, because demodulation is a non-linear process.
- The error decreases if the number of samples per period increases, but it can't be completely solved unless proper synchronization is ensured → <u>restart the ADC</u> <u>conversion whenever any parameter of the DDSs are updated to always sample the</u> <u>input waveform in the same points.</u>



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Experimental demonstration of the heterodyne lock-in

• The effect of the acquisition chain offset is removed with the heterodyne technique.

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Measured voltage [µV] -230 -234 -238 Analog lock-in

RMS noise ~ 2 uV

Time [s]

• The readout noise is reduced because the 1/f component is avoided.

- White noise = $200 \text{nV} / \sqrt{\text{Hz}}$
- 1/f noise corner frequency of the acquisition chain = 10 Hz
- Lock-in bandwidth = 10 Hz
- Intermediate frequency = 5 kHz



- Choose the best lock-in architecture depending on the requirements of the application.
- Beware of 1/f noise after analog demodulation to obtain the best performance.
- Carefully design the signal processing chain of digital LIAs.
- Consider hybrid lock-in solutions in those situations where the standard approaches struggle.

